Lectures on Memory Interface

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Lecture 1
Microprocessor and Memory
Microprocessor Based Computer Systems

FIGURE 1–6  The block diagram of a microprocessor-based computer system.
Memory

- The **memory system** is divided into three main parts:
  - TPA (transient program area): holds the DOS (disk operating system) operating system and other programs that control the computer.
  - System area: contains programs on a read-only memory (ROM) or flash memory, and areas of read/write (RAM) memory for data storage.

![Memory System Diagram]

- TPA: 640K bytes
- System area: 384K bytes
- Extended memory

- 15M bytes in the 80286 or 80386SX
- 31M bytes in the 80386SL/SLC
- 63M bytes in the 80386EX
- 4095M bytes in the 80386DX, 80486, and Pentium
- 64G bytes in the Pentium Pro, Pentium II, Pentium III, Pentium 4, and Core2

- 1M bytes of real (conventional) memory
I/O systems

• The I/O (input/output) space in a computer system extends from I/O port 0000H to port FFFFH (may be 8-bit or 16-bit).

• I/O port address is similar to a memory address, except that instead of addressing memory, it addresses an I/O device.

• The I/O devices allow the microprocessor to communicate between itself and the outside world.

• The I/O space allows the computer to access up to 64K different 8-bit I/O devices, 32K different 16-bit devices, or 16K different 32-bit devices.

FIGURE 1–11 Some I/O locations in a typical personal computer.
Busses

• A bus is a common group of wires that interconnect components in a computer system.

• The buses transfer address, data, and control information between the microprocessor and its memory and I/O systems.

• Three buses exist for this transfer of information:
  – Address
  – Data Bus,
  – Control signals Bus.
Microprocessor CPU

- Is the controlling element in a computer system.
- controls memory and I/O through a series of connections called buses.
- The buses select an I/O or memory device, transfer data between an I/O device or memory and the CPU, and control the I/O and memory system.
- Memory and I/O are controlled through instructions that are stored in the memory and executed by the CPU.
- The CPU performs three main tasks:
  - data transfer between itself and the memory or I/O systems.
  - simple arithmetic and logic operations
  - program flow via simple decisions.
- The power of the CPU is in its capability to execute billions of millions of instructions per second from a program or software (group of instructions) stored in the memory system.
FIGURE 1–12 The block diagram of a computer system showing the address, data, and control bus structure.
Intel 8086 Programming model

• The programming model of the 8086 through the Core2 is considered to be **program visible** (registers are used during application programming and are specified by the instructions).

• Some registers, detailed later in this chapter, are considered to be **program invisible** (are not addressable directly during applications programming) but may be used indirectly during system programming.

• Only the 80286 and above contain the program-invisible registers used to control and operate the protected memory system and other features of the microprocessor.
**Intel 8086 Programming model**

**FIGURE 2–1** The programming model of the 8086 through the Core2 microprocessor including the 64-bit extensions.
Intel 8086 Programming model

- The programming model contains 8, 16, and 32-bit registers. And some contains 64-bit registers when operated in the 64-bit mode.

- The **8-bit registers** are AH, AL, BH, BL, CH, CL, DH, and DL and are referred using two-letter designations (**ADD AL,AH** instruction adds the 8-bit contents of AH to AL, only AL changes due to instruction.)

- The **16-bit registers** are AX, BX, CX, DX, SP, BP, DI, SI, IP, FLAGS, CS, DS, ES, SS, FS, and GS. Some of them consists of tow 8-bit registers (AX=AH + AL).

- The 16-bit registers are referenced with the two-letter designations such as AX (**ADD DX, CX** instruction adds the 16-bit contents of CX to DX, Only DX changes due to this instruction).

- The **extended 32-bit registers** are EAX, EBX, ECX, EDX, ESP, EBP, EDI, ESI, EIP, and EFLAGS. These 32-bit extended registers, and 16-bit registers FS and GS( **ADD ECX, EBX** adds the 32-bit contents of EBX to ECX , Only ECX changes due to this instruction).
Intel 8086 Programming model

- **General-purpose registers:**
  - include EAX, EBX, ECX, EDX, EBP, EDI, and ESI.
  - Hold various data sizes (bytes, words, or double words) and are used for almost any purpose, as dictated by a program.
  - RAX (accumulator), RBX (base index),

- **Special Purpose registers**
  - include RIP, RSP, and RFLAGS; and the segment registers include CS, DS, ES, SS, FS, and GS.
  - RIP (instruction register), RSP (Stack pointer), RFLAGS (indicate the condition of the microprocessor and control its operation such as (C carry), (P parity), (Z zero), (S Sign), (I interrupt), (O Overflow)),......

*FIGURE 2–2* The EFLAG and FLAG register counts for the entire 8086 and Pentium microprocessor family.
Chapter Objectives

• how to interface:
  • Explain how to interface both RAM and ROM to a microprocessor.
  • Memory to an 8-, 16-, 32-, and 64-bit data bus by using various memory address sizes.
• Decode the memory address and use the outputs to select various memory components.
• Use programmable logic devices (PLDs) to decode memory addresses.
• Explain how error correction code (ECC) is used with memory.
• Explain the operation of a dynamic RAM controller.
• Interface dynamic RAM to the microprocessor
Introduction

- Every microprocessor-based system has a memory system.
- There are two main types of memory:
  - **Read-Only memory (ROM).** contains system software and permanent system data.
  - **Random Access Memory (RAM)** or read/write memory, contains temporary data and application software.
- This allows virtually any microprocessor to be interfaced to any memory system.
Common Types of Memory Devices

• There are four common types of memory:
  – read-only memory (ROM)
  – flash memory (EEPROM)
  – static random access memory (SRAM)
  – dynamic random access memory (DRAM).
Computer Memory

- Computers employ many different types of memory to hold data and programs.
  - Semi-conductor Memories
  - magnetic disks, USB sticks, DVDs etc.)
- Each type has its own characteristics and uses.
Memory Hierarchy

- For the same price:
  - CPU processing speed (the number of instructions executed per second) has doubled every 18 months.
  - Computer memory has quadrupling in size every 36 months.
  - Memory speed, has increased at a rate of less than 10% per year.
  - A gap between the speed of the processor and the speed of memory also increases.
Memory Hierarchy

- A computer have several types of memory, ranging from fast, expensive internal registers, to slow, inexpensive Hard Magnetic Disks.
- **Registers:**
  - are matched in speed to the CPU
  - consume a significant amount of power.
  - only a small number of registers in a processor
  - more expensive.
- **Secondary storage:**
  - such as hard magnetic disks.
  - the cost per stored bit is small in terms of money and electrical power.
  - Access time is very long when compared with registers.
- Between the registers and secondary storage there are a number of other forms of memory that bridge the gap between the two.
Memory Hierarchy

- The memory hierarchy can be characterized by a number of parameters:
  - **Access Type**: how physically the memory read/write is done (Random or Sequential).
  - **Capacity** measured in bytes or KB or MB.
  - **Cycle time**: the time elapsed from the start of a read operation to the start of a next read.
  - **Latency** is defined as the time interval between the request for information and the access to the first bit of that information.
  - **Bandwidth**: the number of bits that can be accessed in one second.
  - **Cost** of a memory is usually specified as dollars/MB
  - **Total Cost** = \( \text{cost/MB} \times \text{Memory Size} \).
Typical memory hierarchy

<table>
<thead>
<tr>
<th>Memory Hierarchy Parameters</th>
<th>Access type</th>
<th>Capacity</th>
<th>Latency</th>
<th>Bandwidth</th>
<th>Cost/MB</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU registers</td>
<td>Random</td>
<td>64–1024 bytes</td>
<td>1–10 ns</td>
<td>System clock rate</td>
<td>High</td>
</tr>
<tr>
<td>Cache memory</td>
<td>Random</td>
<td>8–512 KB</td>
<td>15–20 ns</td>
<td>10–20 MB/s</td>
<td>$500</td>
</tr>
<tr>
<td>Main memory</td>
<td>Random</td>
<td>16–512 MB</td>
<td>30–50 ns</td>
<td>1–2 MB/s</td>
<td>$20–50</td>
</tr>
<tr>
<td>Disk memory</td>
<td>Direct</td>
<td>1–20 GB</td>
<td>10–30 ms</td>
<td>1–2 MB/s</td>
<td>$0.25</td>
</tr>
<tr>
<td>Tape memory</td>
<td>Sequential</td>
<td>1–20 TB</td>
<td>30–10,000 ms</td>
<td>1–2 MB/s</td>
<td>$0.025</td>
</tr>
</tbody>
</table>
## The Memory Hierarchy

Typical Cost = \( \text{Cost/MB} \times \text{Typical Amount} \)

<table>
<thead>
<tr>
<th>Memory type</th>
<th>Access time</th>
<th>Cost/MB</th>
<th>Typical amount used</th>
<th>Typical cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Registers</td>
<td>0.5 ns</td>
<td>High</td>
<td>2 KB</td>
<td>–</td>
</tr>
<tr>
<td>Cache</td>
<td>5–20 ns</td>
<td>$80</td>
<td>2 MB</td>
<td>$160</td>
</tr>
<tr>
<td>Main memory</td>
<td>40–80 ns</td>
<td>$0.40</td>
<td>512 MB</td>
<td>$205</td>
</tr>
<tr>
<td>Disk memory</td>
<td>5 ms</td>
<td>$0.005</td>
<td>40 GB</td>
<td>$200</td>
</tr>
</tbody>
</table>
The diagram illustrates the relationship between different types of computer storage devices and their characteristics:

- **Registers**: Fastest, but most expensive and have the smallest capacity.
- **Cache**: Faster than RAM, but less expensive than registers.
- **RAM**: Faster than hard disk, with moderate cost and capacity.
- **Hard Disk**: Slower, but least expensive and has the largest capacity.

The diagram also shows the relationship between speed and flexibility/usability:

- **SPEED**: Faster devices are slower in price and capacity.
- **FLEXIBILITY USABILITY**: Easier to use, but harder to store data.

The cost, capacity, and volatility of each device are also indicated:

- **Cost**: Registers are expensive, RAM is moderate, hard disk is cheap.
- **Capacity**: Registers have small capacity, RAM has moderate capacity, hard disk has large capacity.
- **Volatility**: Registers have high volatility, RAM has moderate volatility, hard disk has low volatility.

The diagram is a useful way to compare and contrast different storage options based on their performance and cost characteristics.
The Memory Hierarchy

- **Registers**
  - Access Time: 1ns → 2ns
- **Level 1 Cache**
  - Access Time: 3ns → 10ns
- **Level 2 Cache**
  - Access Time: 25ns → 50ns
- **Main Memory**
  - Access Time: 30ns → 90ns
- **Fixed Rigid Disk**
  - Access Time: 5ms → 20ms
- **Optical Disk (Jukeboxes)**
  - Access Time: 100ms → 5s *
- **Magnetic Tape (Robotic Libraries)**
  - Access Time: 10s → 3m *

* If volume is mounted.
Memory Hierarchy

• Memory terminology:
  • **Hit**: The requested data resides in a given level of memory.
  • **Miss**: The requested data is not found in the given level of memory.
  • **Hit rate**: The percentage of memory accesses found in a given level of memory.
  • **Miss rate**: The percentage of memory accesses not found in a given level of memory.

\[
\text{Miss Rate} = 1 - \text{Hit Rate.}
\]

• **Hit time**: The time required to access the requested information in a given level of memory.
Memory Hierarchy

- The processor makes a request for an item in memory as follows:
  - The CPU tries to find the item in the first memory level of the memory hierarchy with hit ratio=$h_1$ or miss ratio=$1-h_1$.
  - In case of miss, CPU tries to find the item in the second memory level with hit ratio, $h_2$ or miss ratio = $1-h_2$.
  - The process is repeated until the item is found.
  - In three levels memory hierarchy, the average memory access time can be expressed as follows:

\[
t_{av} = h_1 \times t_1 + (1 - h_1)[t_1 + h_2 \times t_2 + (1 - h_2)(t_2 + t_3)]
\]

\[= t_1 + (1 - h_1)[t_2 + (1 - h_2)t_3]\]

- $t_1$, $t_2$, $t_3$ represent, the access times of the three levels
Main Memory

• The Figure shows an interface between the main memory and the CPU using two CPU registers:

• **MAR** (Memory Address Register): used to store the address of specific location.

• **MDR** (Memory Data Register): used to hold the data to be stored and/or retrieved in/from the memory location.
Main Memory Internal Structure

• Main memory consists of:
  • rows and columns of basic cells that store one bit of information.
  • **Cells** in one row can be used to form a **memory word**.
  • **Address lines** $A_{n-1}A_{n-2} \ldots A_1A_0$ are used as inputs to the address decoder in order to generate the word select lines $W_{2^n-1} \ldots W_1W_0$.
  • A given word select line is common to all memory cells in the same row and is used to enable all cells in a row for read or write.
  • **Data (bit) lines** are used to input or output the contents of cells. Each memory cell is connected to two data lines. A given data line is common to all cells in a given column.
2-1/2D Organization of a 64-Word by One-Bit RAM

Row Decoder

Column Decoder (MUX/DEMUX)

One Stored Bit

Read/Write Control

Read

Data

Column

In/Out

Select

Two bits wide:
One bit for data and
one bit for select.

Data

A₀

A₁

A₂

A₃

A₄

A₅
A conceptual internal organization of a memory chip

Main Memory Internal Structure

Data Lines
Memory Pin connections

- All Memory devices have the following pins:
  - Address input Pins
  - Data input/output Pins
  - Selection input Pins
  - Control input Pins

![Diagram of Memory Chip](image)
Address Connections

• Used to select a memory location within the device.
• Labeled from A₀ (least significant address input), to Aₙ₋₁ where n can be any value.
• No. of address pins = Log₂(Memory Locations)
• No. of Memory Locations = 2^(Address Pins)
• A 1K memory device has 1024 memory locations and 10 address pins.
• It takes a 10-bit binary number to select any single location on a 1024-location device.
  • 1024 different combinations
• if a device has 11 address connections, it has 2¹¹ = 2048 bit = 2KB internal memory locations
Address Input Pins

- The number 400H (0100 0000 0000)B represents a 1K-byte section of the memory system.
- If a memory device is decoded to begin at memory address 10000H and it is a 1K device, its last location is at address \((10000H + 400H) - 1H = 103FFH\)—one location less than 400H.
- 1000H is 4K. A memory device that contains a starting address of 14000H that is 4K bytes long ends at location 14FFFFH—one location less than 1000H.
- A third number is 64K, or 10000H. A memory that starts at location 30000H and ends at location 3FFFFFH is a 64K-byte memory.
Data Connections

• All memory devices have a set of data outputs or input/outputs (bidirectional common I/O pins).
• Data connections are points at which data are entered for storage (WRITE) or extracted for reading.
• Data pins are labeled D0 through D7 for an 8-bit-wide memory device (byte-wide memory). Most devices are 8 bits wide, some are 16 bits, 4 bits, or just 1 bit wide.
• A memory device with 1K memory locations and 8 bits in each location is often listed as a 1K × 8 by the manufacturer.
• Memory devices are often classified according to total bit capacity.
Selection Connections

- Each memory device has an input that selects or enables the memory device (sometimes more than one)
- This type of input is most often called a **Chip Select (CS)** Chip Enable (CE) or simply Select (S) input.
- RAM memory generally has at least one or tow inputs, and ROM has at least one
- If more than one CE connection is present, all must be activated to read or write data.
Control Connections

- **ROM usually has one control input OE (Output Enable)**
  - allows data flow from output data pins.
  - The OE enables and disables a set of three-state buffers located in the device and must be active to read data.

- **RAM has either one or two control inputs:**
  - if one control input, it is often called **R/W (Read / Write)**
  - If the RAM has two control inputs:
    - **WE** write enable must be active to perform memory write.
    - **OE** Output Enable must be active to perform a memory read
  - when the two controls are present, they must never both be active at the same time
  - If both inputs are inactive, data are neither written nor read. the connections are at their high-impedance state.
Main Memory Cell

- Each main memory cell consists of six CMOS transistors. The six transistor static CMOS memory cell consists of two inverters back to back.
Main Memory Cell

Read operation:

1. Both lines $b$ and $\bar{b}$ are precharged high.
2. The word select line is activated, thus turning on both transistors $N_3$ and $N_4$.
3. Depending on the internal value stored in the cell, point $A(B)$ will lead to the discharge of line $b(\bar{b})$.

Write operation:

1. The bit lines are precharged such that $b(\bar{b}) = 1(0)$.
2. The word select line is activated, thus turning on both transistors $N_3$ and $N_4$.
3. The bit line precharged with 0 will have to force the point $A(B)$, which has 1, to 0.
Memory Design

- Design a 1KX4 memory chip.
- It can be designed as where \( n = 10 \), 1K rows of cells, each consisting of four cells. The chip will then have to have 10 pins for the address and four pins for the data.
- This not the Best utilization of chip area.
Memory Design Factors

- Design a 1KX4 memory chip.
- It can be designed as 64 rows, each consisting of 64 cells. In this case, 6 address lines forming the row address.
- The remaining 4 address lines (column address) will be used to select the appropriate 4 bits among the available 64 bits constituting a row.
Memory Design

- Design a 4k bits memory chip.
- Different organization of the same memory capacity can lead to a different number of chip pins requirement.

<table>
<thead>
<tr>
<th>Organization</th>
<th>Number of needed address lines</th>
<th>Number of needed data lines</th>
</tr>
</thead>
<tbody>
<tr>
<td>4K×1</td>
<td>12</td>
<td>1</td>
</tr>
<tr>
<td>1K×4</td>
<td>10</td>
<td>4</td>
</tr>
<tr>
<td>512×8</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>256×16</td>
<td>8</td>
<td>16</td>
</tr>
</tbody>
</table>

- It is clear from the table that increasing the number of bits per addressable location results in an increase in the number of pins needed in the integrated circuit.
Random Access Memory

- Random means that any memory location can be accessed in the same amount of time, regardless of its position in the memory.
- D flip-flop, with additional controls to allow the cell to be selected, read, and written. There is a (bidirectional) data line for data input and output.

Static RAM cell (a) and dynamic RAM cell (b).
• A Four-Word Memory with Four Bits per Word in a 2D Organization.
• A Simplified Representation of the Four-Word by Four-Bit RAM

![Simplified Diagram](image)

• Creating a Four-Word by Eight-Bit RAM using Two Four-Word by Four-Bit RAMs.

![Diagram](image)
Two Four-Word by Four-Bit RAMs Make up an Eight-Word by Four-Bit RAM
ROM Memory

- The **read-only memory** (ROM):
  - permanently stores programs and data that are resident to the system and must not change when power supply is disconnected. The ROM is permanently programmed
  - **non-volatile memory**, because its contents *do not* change even if power is disconnected.

- Today, the ROM is available in many forms.

- A device we call a ROM is purchased in mass quantities from a manufacturer and programmed during its fabrication at the factory.
ROM Memory (EPROM and PROM)

- The EPROM (erasable programmable read-only memory), a type of ROM, is more commonly used when software must be changed often or when too few are in demand to make the ROM economical.

- An EPROM is programmed in the field on a device called an EPROM programmer. The EPROM is also erasable if exposed to high-intensity ultraviolet light for about 20 minutes or so, depending on the type of EPROM.

- The PROM (programmable read-only memory) is also programmed in the field by burning open tiny Ni-chrome or silicon oxide fuses; but once it is programmed, it cannot be erased.
ROM Memory (Flash Memory)

- The flash memory is also often called an EEPROM (electrically erasable programmable ROM), or a NOVRAM (non-volatile RAM).
  - Are electrically erasable in the system, but they require more time to erase than a normal RAM.
  - The flash memory device is used to store setup information for systems such as the video card in the computer.
  - It has all but replaced the EPROM in most computer systems for the BIOS memory.
  - Some systems contain a password stored in the flash memory device.
  - Flash memory has its biggest impact in memory cards for digital cameras and memory in MP3 audio players.
FIGURE 10–2  The pin-out of the 2716, 2K × 8 EPROM. (Courtesy of Intel Corporation.)
A ROM Stores Four Four-Bit Words
ROM Memory (Flash Memory)

- Data appear on the output connections only after a logic 0 is placed on both $CE$ and $OE$ pin connections.
- If $CE$ and $OE$ are not both logic 0s, the data output connections remain at their high-impedance or off states.
- Note that the $V_{PP}$ pin must be placed at a logic 1 level for data to be read from the EPROM.
- In some cases, the $V_{PP}$ pin is in the same position as the $WE$ pin on the SRAM.
- This will allow a single socket to hold either an EPROM or an SRAM.
FIGURE 10–3 The timing diagram of AC characteristics of the 2716 EPROM. (Courtesy of Intel Corporation.)
ROM Memory (Flash Memory)

A.C. Characteristics

\[ T_A = 0^\circ C \text{ to } 70^\circ C, \ V_{CC}^{[1]} = +5V \pm 5\%, \ V_{PP}^{[2]} = V_{CC} \pm 0.6V^{[3]} \]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
<tr>
<td>( t_{ACC1} )</td>
<td>Address to Output Delay</td>
<td>250</td>
<td>450</td>
<td></td>
</tr>
<tr>
<td>( t_{ACC2} )</td>
<td>PD/PGM to Output Delay</td>
<td>280</td>
<td>450</td>
<td></td>
</tr>
<tr>
<td>( t_{CO} )</td>
<td>Chip Select to Output Delay</td>
<td>120</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{PF} )</td>
<td>PD/PGM to Output Float</td>
<td>0</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>( t_{DF} )</td>
<td>Chip Deselect to Output Float</td>
<td>0</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>( t_{OH} )</td>
<td>Address to Output Hold</td>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Capacitance\(^{[5]}\) \( T_A = 25^\circ C, \ f = 1 \text{ MHz} \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_{IN} )</td>
<td>Input Capacitance</td>
<td>4</td>
<td>6</td>
<td>pF</td>
<td>( V_{IN} = 0V )</td>
</tr>
<tr>
<td>( C_{OUT} )</td>
<td>Output Capacitance</td>
<td>8</td>
<td>12</td>
<td>pF</td>
<td>( V_{OUT} = 0V )</td>
</tr>
</tbody>
</table>

A.C. Test Conditions:
- Output Load: 1 TTL gate and \( C_L = 100 \text{ pF} \)
- Input Rise and Fall Times: \( \leq 20 \text{ ns} \)
- Input Pulse Levels: 0.8V to 2.2V
- Timing Measurement Reference Level:
  - Inputs: 1V and 2V
  - Outputs: 0.8V and 2V
Flash Memory

(a) External view of flash memory module and (b) flash module internals. (Source: adapted from HowStuffWorks.com.)
Memory Access Time

- Memory access time $T_{\text{ACC}}$—the time that it takes the memory to read information. $T_{\text{ACC}}$ is measured from the appearance of the address at the address inputs until the appearance of the data at the output connections.
- This is based on the assumption that the $\overline{CE}$ input goes low at the same time that the address inputs become stable. Also, $\overline{OE}$ must be a logic 0 for the output connections to become active.
- The basic speed of EPROM is 450 ns. And 086/8088 operated with a 5 MHz clock allowed memory 460 ns to access data.
- Wait states are required to operate properly with the 8086/8088 microprocessors.
Static RAM Devices

- is a RAM chips that are based upon flip-flops, because the contents of each location persist as long as power is applied to the chips.

- Static RAM memory devices retain data for as long as DC power is applied. Because no special action (except power) is required to retain stored data, these devices are called static memory.

- They are also called volatile memory because they will not retain data without power.

- The SRAM, which stores temporary data, is used when the size of the read/write memory is relatively small.
Static RAM Devices

FIGURE 10–4  The pin-out of the TMS4016, 2K × 8 static RAM (SRAM). (Courtesy of Texas Instruments Incorporated.)
## Static RAM Devices

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP†</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$ High level voltage</td>
<td>$I_{OH} = -1 \text{ mA,}$ $V_{CC} = 4.5 \text{ V}$</td>
<td>2.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$ Low level voltage</td>
<td>$I_{OL} = 2.1 \text{ mA,}$ $V_{CC} = 4.5 \text{ V}$</td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{I}$ Input current</td>
<td>$V_{I} = 0 \text{ V to 5.5 \text{ V}}$</td>
<td>10</td>
<td></td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_{OZ}$ Off-state output current</td>
<td>$S$ or $G$ at 2 \text{ V or $W$ at 0.8 \text{ V,}}$ $V_{O} = 0 \text{ V to 5.5 \text{ V}}$</td>
<td>10</td>
<td></td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_{CC}$ Supply current from $V_{CC}$</td>
<td>$I_{O} = 0 \text{ mA,}$ $T_{A} = 0\degree \text{ C (worst case)}$ $V_{CC} = 5.5 \text{ V}$</td>
<td>40</td>
<td>70</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$C_{I}$ Input capacitance</td>
<td>$V_{I} = 0 \text{ V,}$ $f = 1 \text{ MHz}$</td>
<td>8</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$C_{O}$ Output capacitance</td>
<td>$V_{O} = 0 \text{ V,}$ $f = 1 \text{ MHz}$</td>
<td>12</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

†All typical values are at $V_{CC} = 5 \text{ V, } T_{A} = 25\degree \text{ C.}$

Timing requirements over recommended supply voltage range and operating free-air temperature range

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TMS4016-12</th>
<th>TMS4016-15</th>
<th>TMS4016-20</th>
<th>TMS4016-25</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{c(rd)}$ Read cycle time</td>
<td>120</td>
<td>150</td>
<td>200</td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{c(wr)}$ Write cycle time</td>
<td>120</td>
<td>150</td>
<td>200</td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{w(W)}$ Write pulse width</td>
<td>60</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{su(A)}$ Address setup time</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{su(S)}$ Chip select setup time</td>
<td>60</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{su(D)}$ Data setup time</td>
<td>50</td>
<td>60</td>
<td>80</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{H(A)}$ Address hold time</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{H(D)}$ Data hold time</td>
<td>5</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>ns</td>
</tr>
</tbody>
</table>
Static RAM Devices

timing waveform of read cycle (see note 5)
Static RAM Devices

timing waveform of write cycle no. 1 (see note 6)
# Static RAM Devices

Switching characteristics over recommended voltage range, $T_A = 0^\circ C$ to $70^\circ C$

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TMS4016-12</th>
<th>TMS4016-15</th>
<th>TMS4016-20</th>
<th>TMS4016-25</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{a(A)}$ Access time from address</td>
<td>120</td>
<td>150</td>
<td>200</td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{a(S)}$ Access time from chip select low</td>
<td>60</td>
<td>75</td>
<td>100</td>
<td>120</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{a(G)}$ Access time from output enable low</td>
<td>50</td>
<td>60</td>
<td>80</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{v(A)}$ Output data valid after address change</td>
<td>10</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{dis(S)}$ Output disable time after chip select high</td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>80</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{dis(G)}$ Output disable time after output enable high</td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>80</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{dis(W)}$ Output disable time after write enable low</td>
<td>50</td>
<td>60</td>
<td>60</td>
<td>80</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{en(S)}$ Output enable time after chip select low</td>
<td>5</td>
<td>5</td>
<td>10</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{en(G)}$ Output enable time after output enable low</td>
<td>5</td>
<td>5</td>
<td>10</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{en(W)}$ Output enable time after write enable high</td>
<td>5</td>
<td>5</td>
<td>10</td>
<td>10</td>
<td>ns</td>
</tr>
</tbody>
</table>

**NOTES:**
3. $C_L = 100pF$ for all measurements except $t_{dis(W)}$ and $t_{en(W)}$.
   $C_L = 5pF$ for $t_{dis(W)}$ and $t_{en(W)}$.
4. $t_{dis}$ and $t_{en}$ parameters are sampled and not 100% tested.

**FIGURE 10–5** (a) The AC characteristics of the TMS4016 SRAM. (b) The timing diagrams of the TMS4016 SRAM. (Courtesy of Texas Instruments Incorporated.)
Dynamic RAM Devices DRAM

- The same as SRAM, except that it retains data for only 2 or 4 ms on an integrated capacitor. After 2 or 4 ms, the contents of the DRAM must be completely rewritten \textit{(refreshed)} because the capacitors, which store a logic 1 or logic 0, lose their charges.

- Refresh is reading the content of memory location and write it again which is impossible task. This occurs during write, read or during special refresh cycle.

- The manufacturer has internally constructed the DRAM differently from the SRAM. So that, the entire content of the memory are refreshed with 256 reads in a 2- 4-ms.

- DRAM requires so many address pins that the manufacturers have decided to multiplex the address inputs.
Dynamic RAM Devices DRAM

- Is a RAM chips, employ a capacitor, which stores a minute amount of electric charge, in which the charge level represents a 1 or a 0.
- Capacitors are much smaller than flip-flops, so a capacitor based DRAM can hold much more information in the same area than an SRAM.
- Since the charges on the capacitors dissipate with time, the charge in the capacitor storage cells in DRAMs must be restored, or refreshed frequently.
Dynamic RAM Devices DRAM

A₀ - A₁₄  
I₀₁₀ - I₀₇  
CS  
OE  
WE  
V_C  
GND 

Addresses  
Data connections  
Chip select  
Output enable  
Write enable  
+5V Supply  
Ground

**FIGURE 10–7** The pin-out of the TMS4464, 64K × 4 dynamic RAM (DRAM).  
(Courtesy of Texas Instruments Incorporated.)

(a)  

PIN NOMENCLATURE

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A₀-A₇</td>
<td>Address Inputs</td>
</tr>
<tr>
<td>CAS</td>
<td>Column Address Strobe</td>
</tr>
<tr>
<td>DQ₁-DQ₄</td>
<td>Data-In/Data-Out</td>
</tr>
<tr>
<td>G</td>
<td>Output Enable</td>
</tr>
<tr>
<td>RAS</td>
<td>Row Address Strobe</td>
</tr>
<tr>
<td>V_DD</td>
<td>+5-V Supply</td>
</tr>
<tr>
<td>V_SS</td>
<td>Ground</td>
</tr>
<tr>
<td>W</td>
<td>Write Enable</td>
</tr>
</tbody>
</table>
Dynamic RAM Devices DRAM

- A DRAM 64K × 4 DRAM, which stores 256K bits of data. Can use only eight address inputs instead of 16—the number required to address 64K memory locations.

- The Multiplexing operation requires two special pins: the column address strobe (CAS) and row address strobe (RAS).

- First, A0–A7 are placed on the address pins and strobed into an internal row latch by RAS as the row address.

- Next, the address bits A8--A15 are placed on the same eight address inputs and strobed into an internal column latch by CAS as the column address.

- The 16-bit address held in these internal latches addresses the contents of one of the 4-bit memory locations.
Dynamic RAM Devices DRAM

FIGURE 10–9  Address multiplexer for the TMS4464 DRAM.
Dynamic RAM Devices DRAM

FIGURE 10–8  RAS, CAS, and address input timing for the TMS4464 DRAM. (Courtesy of Texas Instruments Incorporated.)
Dynamic RAM Devices DRAM

- DRAM memory is often placed on small circuit boards called SIMMs (Single In-Line Memory Modules).
- The 30-pin SIMM is organized most often as 1M × 8 or 1M × 9, and 4M × 8 or 4M × 9.
- The ninth bit is the parity bit.
- Also shown is a newer 72 pin SIMM. The 72-pin SIMMs are often organized as 1M × 32 or 1M × 36 (with parity).
- Other sizes are 2M × 32, 4M × 32, 8M × 32, and 16M × 32. These are also available with parity.
Dynamic RAM Devices DRAM

- Pentium 4 microprocessors have a 64-bit wide data bus,
- SIMMs must be used in pairs to obtain a 64-bit-wide data connection.
- Today, the 64-bit-wide DIMMs (Dual In-line Memory Modules) have become the standard in most systems.
- The memory on these modules is organized as 64 bits wide. The common sizes available are 16M bytes (2M × 64), 32M bytes (4M × 64), 64M bytes (8M × 64), 128M bytes (16M × 64), 256M bytes (32M × 64), 512M bytes (64M × 64), and 1G bytes (128M × 64).
FIGURE 10–11 The pin-outs of the 30-pin and 72-pin SIMM. (a) A 30-pin SIMM organized as $4M \times 9$ and (b) a 72-pin SIMM organized as $4M \times 36$. 

Dynamic RAM Devices DRAM
Dynamic RAM Devices DRAM

FIGURE 10–12 The pin-out of a 168-pin DIMM.
1. What types of connections are common to all memory devices?

2. List the number of words found in each memory device for the following numbers of address connections:
   (a) 8     (b) 11     (c) 12     (d) 13     (e) 20

3. List the number of data items stored in each of the following memory devices and the number of bits in each datum:
   (a) 2K × 4     (b) 1K × 1     (c) 4K × 8     (d) 16K × 1     (e) 64K × 4

4. What is the purpose of the $\overline{CS}$ or $\overline{CE}$ pin on a memory component?

5. What is the purpose of the $\overline{OE}$ pin on a memory device?

6. What is the purpose of the $\overline{WE}$ pin on a SRAM?

7. How many bytes of storage do the following EPROM memory devices contain?
   (a) 2708     (b) 2716     (c) 2732     (d) 2764     (e) 27512
9. Why won’t a 450 ns EPROM work directly with a 5 MHz 8088?
10. What can be stated about the amount of time needed to erase and write a location in a flash memory device?
11. SRAM is an acronym for what type of device?
12. The 4016 memory has a $\bar{G}$ pin, $\bar{S}$ and $\bar{W}$ pin, and a pin. What are these pins used for in this RAM?
13. How much memory access time is required by the slowest 4016?
14. DRAM is an acronym for what type of device?
15. The 256M DIMM has 28 address inputs, yet it is a 256M DRAM. Explain how a 28-bit memory address is forced into 14 address inputs.
16. What are the purposes of the $\bar{CAS}$ and $\bar{RAS}$ inputs of a DRAM?
17. How much time is required to refresh the typical DRAM?